In the Specification

Delete the paragraph [0010] and replace it with the following paragraph:

[0010] As IC dimensions continue to shrink with future generations of semiconductor technology, these conventional techniques of depositing a barrier or liner layer to fill exposed pores in a porous dielectric layer are becoming increasingly inefficient. This is especially the case wherein exposed pores of the porous dielectric layer reside within via and/or trench openings. As IC dimensions scale down, the dimensions of these via/trench openings also decrease. In so doing, in the process of depositing a barrier liner layer to close exposed pores within via/trench openings, this deposited barrier liner layer undesirably occupies valuable space within these smaller openings. In turn, an insufficient amount of metallurgy will be subsequently depositing into the remaining openings resulting in an ~~undesirably~~ undesirable increase in wire resistance.

Delete the paragraph [0022] and replace it with the following paragraph:

[0022] The in-situ chemical reaction may be allowed to occur for a time sufficient to allow the pore-closing layer grow out laterally from the closed pore to form a liner layer on exposed surfaces of the low-k porous dielectric layer. Alternatively, the liner layer may be formed by allowing the first reactant to absorb within the at least one exposed pore and adsorb onto exposed surfaces

of the low-k porous dielectric layer. The second reactant then contacts the outgassed first reactant at the mouth region and the adsorbed first reactant on the exposed surfaces of the low-k porous dielectric layer to generate the in-situ chemical reaction at the mouth region and at the exposed surfaces of the low-k porous dielectric layer. In so doing, the pore-closing layer is formed across the mouth region and the liner layer is formed on the exposed surfaces of the low-k porous dielectric layer.

Delete the paragraph [0062] and replace it with the following paragraph:

[0062] Dual damascene or single damascene trenches and vias, as discussed above, are formed as known in the art. The present invention provides for closing these exposed pores 35 by first introducing a first reactant, such as, an oxygen-containing surfactant 50 into the chamber, as shown in Fig. 3. For example, water molecules may first be introduced into the chamber. The porous low k dielectric layer may be exposed to the water molecules under processing conditions including pressures ranging from about 1mTorr to about 7,600 Torr, temperatures ranging from ~~about~~ about 50°C to about 450°C, for a time sufficient to at least allow filling the exposed pores 35 with absorbed water molecules, such as a time ranging from about 10 seconds to about 1 hour.

Delete the paragraph [0086] and replace it with the following paragraph:

[0082] Again, this in-situ reaction generates in-situ dielectric molecules that bond together to form an in-situ pore-closing layer 70 across the mouth region 37 inside exposed pores 35 to close off or seal such exposed pores, while retaining porous regions of each exposed pore for maintaining the low dielectric constant (k) of the porous layer 20, as well as providing openings 40 with smooth, planar surfaces for subsequent processing steps. As an alternative to this approach, rather than forming pore-closing layer 70 via treatment with a silane-containing plasma, the structure may be immersed into a solution for formation of the exposed ~~pore-closing~~ pore-closing layer 70 as discussed above.

Delete the paragraph [0104] and replace it with the following paragraph:

[0104] Referring to Figs. 9A-9B, in either event, once the pores 35 are closed via the present pore-closing layer 70 (as shown in Fig. 6), and optionally a bottomless liner layer 90 is formed in addition to the pore-closing layers 70 (as shown in Fig. 8), the resultant structures may be further processed by known metallization steps. In so doing, hard mask layer 24 is removed, and if present, any exposed portions of the cap layer 18 residing within the bottom of via 47 openings are removed by known techniques. Additional barrier/liner layer 12' is conformally deposited within openings 40 such that is coats the sidewalls and bottom surfaces within each of the openings 40. Any remaining empty portions of openings 40 are then filled with additional

metallization layer 14', such as, but not limited to damascene copper, tungsten, aluminum and the like. The resultant structures include a metallized semiconductor structure having the pore sealing layer 70 of the invention (Fig. 9A), and a metallized semiconductor structure having the present ~~invention"s~~invention's bottomless liner 90 in addition to pore sealing layer 70 (Fig. 9B).